Enhancements in CA-UDFM Models to Optimize the Development Flow of Custom Macros/IP and Standard Cell Libraries

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Motivation for cell-aware testing

- Addressing defects within cells requires closer observation within the layout; port-level fault modeling is insufficient, especially for larger and more complex cells.
- Quality of ICs becomes challenging and crucial, particularly in industries like automotive where **lower DPPM** targets are set.
- A SPICE netlist extracted from cell layout with parasitic elements (in **LPE netlist**) provides a much closer physical representation of a cell.
- Defects are emulated based on SPICE LPE netlist elements.
- Example of **defects**: **Bridge/Short** defects occur due to unintended low resistance paths between isolated nodes, causing excessive current flow.
- Open defects arise from spaces or openings in conductors (like metals), preventing current flow.

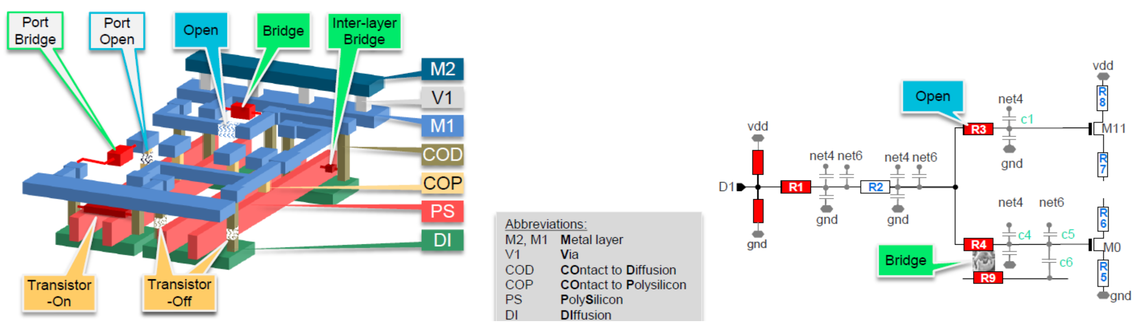
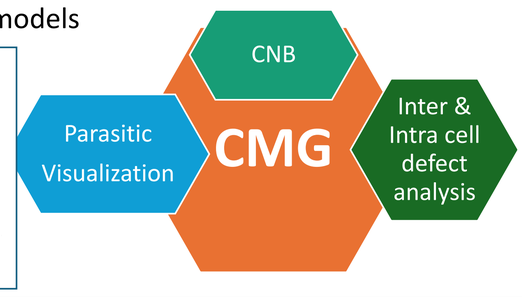


Fig 1: Defect-Oriented Test Overview

Summary of Enhancements

1. **Visualization** of Layout Parasitic Extracted (LPE) netlist to
   - Get overview of design parasitics
     - 3rd party vendor LPE inspection
   - Ensure LPE extraction was done properly by the extraction tool(s)
     - Identify missing power rails, special nets, bridge defects in LPE netlist
2. Identify the **Critical Region** in layout, with high **probability** of finding a **Latent defect**
   - Target Flow: Circuit design → Layout → LPE → UDFM (User Defined Fault Models) for fault analysis
   - Union of **Multiple PVT corner/s** and **RC extraction corner/s** condition specific UDFM patterns to cover all possible Latent defect scenarios
   - Special attention is given to support **complex Macro cells** where probability of finding the defect is high
3. **CNB** (Cell Neighborhood Bridge) support to catch Inter cell defects
   - Set the correct SoC (System on Chip) design specific options and technology specific options to get the correct UDFM models

Conclusion:
- **2X productivity improvement:** CellModelGen **(**CMG) tool reduces design cycle time from weeks to hours
- **Enhanced reliability:** Early identification of latent defects improves Design for Testability (DFT).
- **Effective defect detection:** CNB support catches inter-cell defects, crucial for low DPPM.

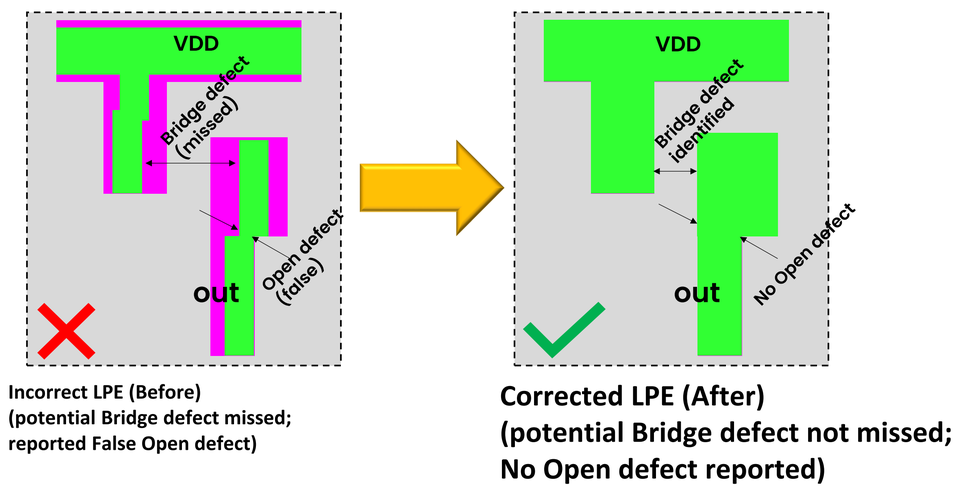


Technical Details on Enhancements

(1) Novel approach to get overview of layout parasitics

- **Visualization** of the LPE netlist is the new approach that we adopted to
  - Ensure that extraction was done properly by standard extraction tools, especially, in 3rd party LPE netlists
    - power rails were not missed, critical nets (e.g. clocks) were correctly extracted
    - potential **Bridge defects not missed,** and **no false Open defects** reported, due to incorrect extraction
  - Overlaying the original layout (GDS) on the visualized view of LPE netlist, helped locate defects
    - **Bridge/Short defect** is created when an unintended low resistance path between isolated nodes causes excessive current flow creating potential **shorts** during manufacturing
    - Space or opening in a conductor (like metals), preventing current flow, leads to **Open defect**

Results:
- Identify issues caused by 3rd party LPE netlists
- Avoid false and missed violations
- Identify and debug issues due to incorrect Extraction of LPE netlist
- LPE netlist is no more a black-box !



Incorrect LPE (Before)
(potential Bridge defect missed; reported False Open defect)

Corrected LPE (After)
(potential Bridge defect not missed; No Open defect reported)

Fig 2: Visualization option to verify LPE netlist

(2) Identify Critical Region, with high probability of finding a Latent defect

- New and innovative approach for identifying Critical R and CC in an LPE, serves as the first step towards locating latent defects. Such defects, defined using new UDFM vectors, are added to existing Reliability test patterns/vectors leading to improvements in DFT

Result:
Critical R and CC values are identified and modified in LPE, then simulated until Latent defects appear. Generate New UDFM vectors based on multiple PVT corners, as patterns are sensitive to PVT and RC extraction corners. Finally, merge the test patterns as per the requirement for future reliability analyses.

Flow adopted:
- Select critical **Reg2Reg** timing paths prone to failure
- Select **critical cell** and **critical timing arc**, on critical timing path
- Identify critical R and CC in LPE netlist where probability of finding Latent defect is high (refer MUX cell example)
- Perform “fault free” SPICE simulation with critical R and CC in LPE (**SIM_A**)
- Perform “faulty” simulation (SPICE): Modify critical R and CC values in LPE and simulate it until the **Latent (Bridge/Open) defect** appears (**SIM_B**)
  - Bridge defect is a function of CC(critical)
  - Open defect is a function of R(critical)
- Compare **SIM_A** and **SIM_B** results to **generate extra UDFM patterns**

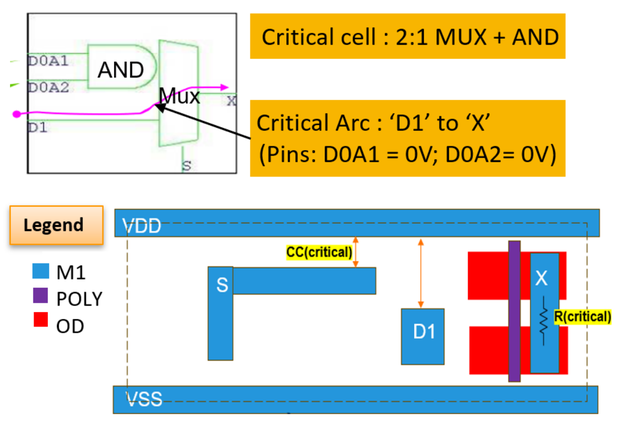


Fig 3: Critical R and CC identified using the CMG tool

(3) CNB support to catch Inter cell defects

- Bridge defect between two adjacent cells
  - Example: A bridge between an internal net of cell 1 and an internal net of cell 2
- These bridges are not targeted by other fault models
  - Node-based fault models like Stuck-at cannot consider such defects
  - Cell-aware UDFM considers only bridges within a cell
  - Interconnect bridges are only related to nets between cell ports
- Increasing probability with smaller distance between the cells, especially in newer technologies
  - Fig. 4 shows a Bridge defect location between two cells (Buffer and Filler cells) in a FinFet technology node
- Chip layout dependent cell pair identification is needed to target such defects

Result:
Identification of the probable Inter cell defect location is made possible by setting technology specific CMG options like for example the maximum distance for potential bridges which maps to the diameter of the bridge defect. This needs close collaboration with Foundry and the it’s cleanroom unit

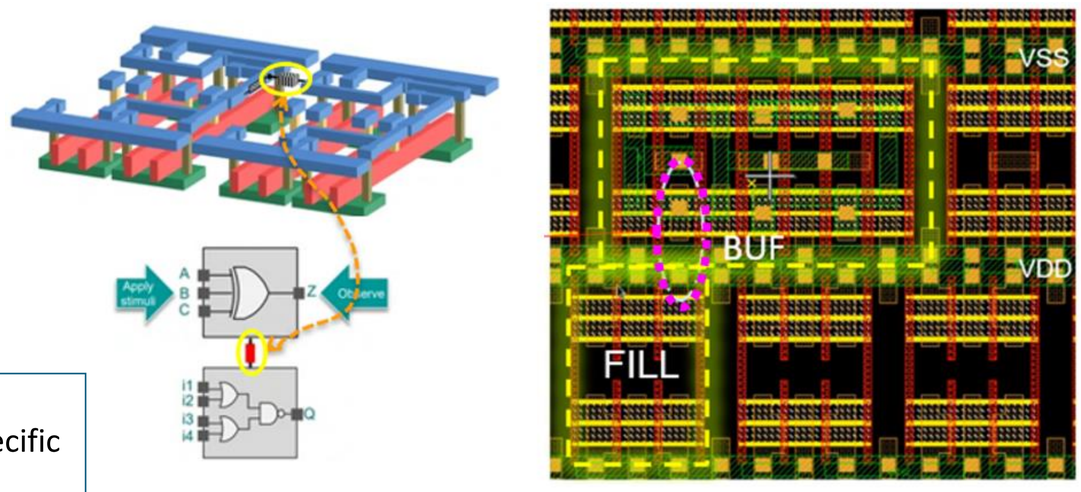


Fig 4: Bridge defect identified in one of the FinFet technology design

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